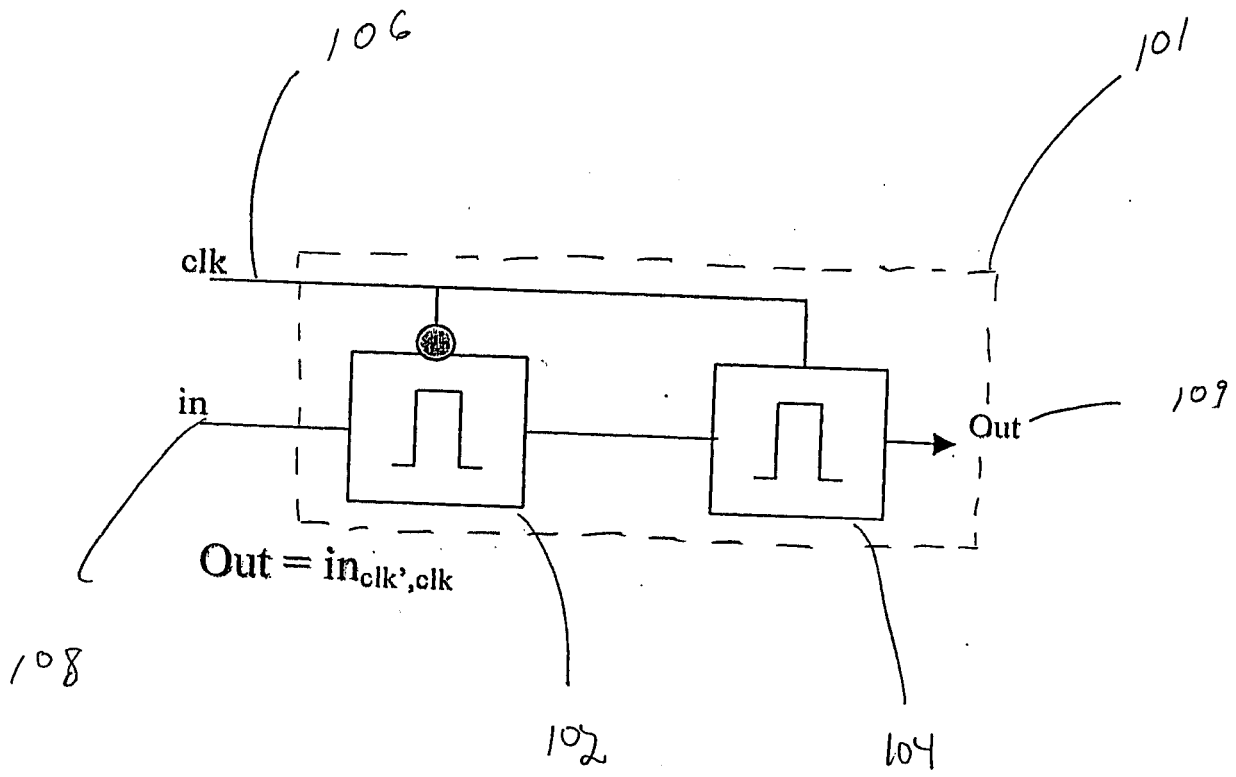

Figure 1

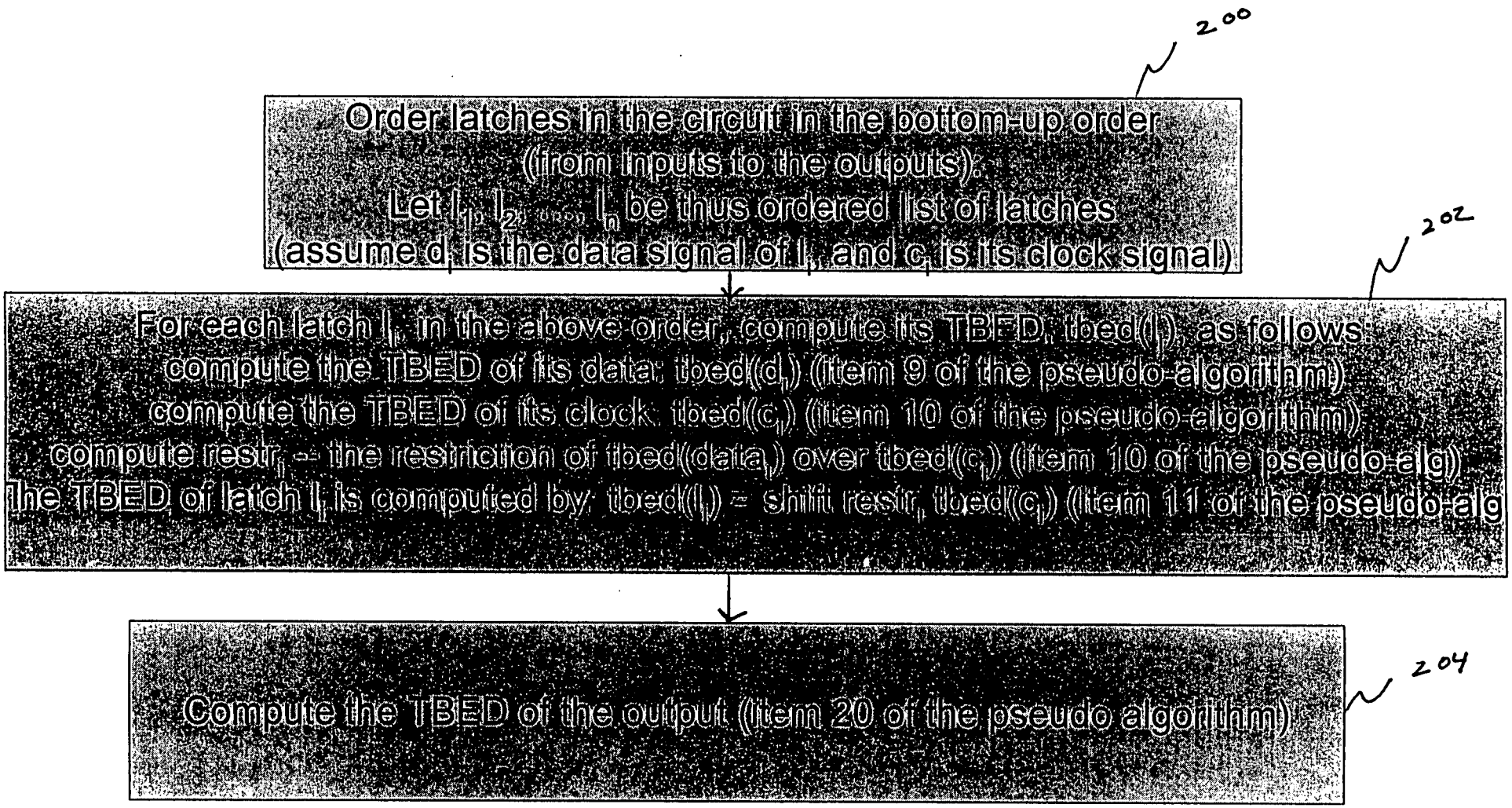
200
Order latches in the circuit in the bottom-up order
(from inputs to the outputs).
Let $l_1, l_2, \ldots, l_n$ be thus ordered list of latches
(assume d_i is the data signal of l_i and c_i is its clock signal)
202
For each latch l_i in the above order, compute its TBED, tbed(l_i), as follows:
compute the TBED of its data: tbed(d_i) (item 9 of the pseudo-algorithm)
compute the TBED of its clock: tbed(c_i) (item 10 of the pseudo-algorithm)
compute $restr_i$ = the restriction of tbed(data$_i$) over tbed(c_i) (item 10 of the pseudo-alg)
The TBED of latch l_i is computed by: tbed(l_i) = shift $restr_i$ tbed(c_i) (item 11 of the pseudo-alg
204
Compute the TBED of the output (item 20 of the pseudo algorithm)

Figure 2

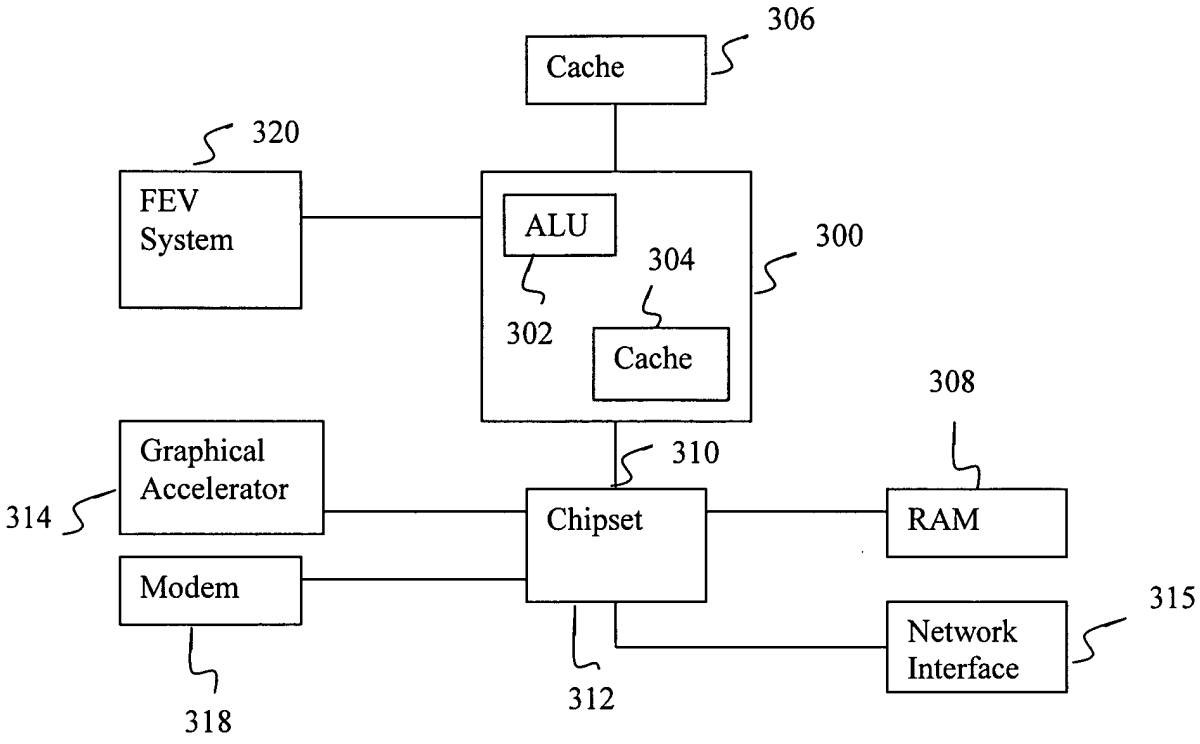
306
Cache
320
FEV
System
ALU
304
300
302
Cache
308
Graphical
Accelerator
310
314
Chipset
RAM
Modem
315
Network
Interface
312
318

Figure 3